## REMARKS

The above amendments and following remarks are submitted in response to the Final Official Action of the Examiner mailed June 17, 2004. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

Claims 11, 14, 16, and 19 have been rejected under 35 U.S.C. 102(b) as being anticipated by newly cited U.S. Patent No. 5,564,035, issued to Lai (hereinafter referred to as "Lai"). This ground of rejection is respectfully traversed as based upon clearly erroneous findings of fact.

Claim 11 is an independent method claim having four steps. These are:

> 1) Formulating a write memory request;
> 2) First experiencing a level one cache memory hit in response to said write memory request;
> 3) Second experiencing a level two cache memory hit in response to said first experiencing step; and
> 4) Invalidating a portion of said level one cache memory corresponding to said write memory request in response to said second experiencing step.

It is clear that this is a process involving the making of a "memory request" by a "local processor", because hits are experienced at the "level one cache memory" and the "level two cache memory". This interpretation is further supported by the structural environment found in the preamble which requires "a level one cache memory of a processor". The claimed "level one

cache memory" is the level one cache memory of and local to the claimed processor.

In making his rejection, the Examiner cites Lai, column 2, lines 48-57. Unlike the claimed experiencing of local processor level one and level two cache memory hits, this citation describes memory bus SNOOPing, concerning the write request of a "remote processor". Lai, column 2, lines 44-48, states:

> For example, L2 cache 203 performs the snooping of memory access requests over system bus 208, which frees the first level cache 202 to be dedicated to interactions with the first processor 200.

The alleged "hits" in L1 and L2 cache memory of the reference result from SNOOPing, rather than from a local write request, as claimed. Furthermore, as a matter of necessity, the SNOOP hits of the reference occur first in the L2 cache memory, whereas the claimed local write request hit is "first experienced" at the L1 cache memory and only "second experienced" at the L2 cache memory. Because this Lai citation describes an example of "SNOOPing" a remote processor request rather than handling the claimed local processor request, it cannot have the claimed "first experiencing" and "second experiencing" steps.

The Examiner specifically acknowledges this clearly erroneous finding of fact in his rejection of claim 1. The Examiner states

> Lai discloses invalidating a corresponding level one cache memory location in response to a <u>non-local</u> write....

Thus, the rejection of claim 11 is based upon clearly erroneous findings of fact and cannot meet the limitations of claim 11. Therefore, the rejection of claim 11, and all claims depending therefrom, is respectfully traversed.

Claim 14 depends from claim 11 and is limited by three additional steps including "recording location of data corresponding to said read memory request." In making his rejection, the Examiner cites Lai column 6, line 45, through column 7, lines 11. However, unlike the claimed invention, Lai discusses recording of a "victim line". Column 6, lines 62-64, states:

> If D=1 of F=1, the victim line is temporarily stored in a victim line buffer (not shown) so that it may be later saved in the next level cache (step 710).

There is no showing that Lai "records the location of data corresponding to read memory request" following a level one cache memory miss.

Furthermore, claim 14 depends from claim 11. Nevertheless, the Examiner has attempted to read claim 11 onto the Background of the Invention of Lai and claim 14 onto the preferred embodiment of Lai, as if the embodiments of column 2, lines 45-57, and column 6, line 45, through column 7, line 11, are somehow the same. These are mutually exclusive embodiments as clearly taught by Lai. Therefore, they cannot be combined as alleged by the Examiner.

As to the prior art embodiment described by Lai, column 3, lines 7-20, states:

> However, a disadvantage of two-level caching under the inclusion policy is that if the ration in size between first level and second level caches is small, much of the second level cache will consist of data that is already in the primary cache.....It is therefore desired to increase the efficiency of a multi-level caching configuration, Specifically in the case when the sizes of caches on adjacent levels are relatively similar.

Thus, Lai actually disparages the embodiment of column 2, lines 45-57, which the Examiner utilizes to reject claim 11, in favor of the mutually exclusive preferred embodiment. Lai distinguishes the later embodiment stating at column 3, lines 24-28:

> The present invention overcomes the disadvantages of the prior art by providing a multi-level cache system in which the higher level cache is treated as an extension of the lower level cache, rather than as containing a duplicate of the lower level cache.

Therefore, Lai clearly teaches that the embodiment of column 2, lines 45-57, and the embodiment of column 6, line 45, through column 7, lines 11, are mutually exclusive and cannot be combined as alleged. The rejection of claim 14 is respectfully traversed.

In his rejection of claim 16, the Examiner again repeats the clearly erroneous finding of fact in citing Lai column 2, lines 52-57. This describes SNOOPing of a remote processor memory request rather than a cache first and second level cache memory misses of a local processor memory request. The rejection of

claim 16, and all claims depending therefrom, is respectfully traversed.

In rejecting claim 19, the Examiner repeats the errors of his rejection of claim 14, including the attempt to combine mutually exclusive embodiments and clearly erroneously finding that the "temporary storage of the victim line" is the same as "recording location of data in response to a level one cache read miss". Furthermore, the Examiner misquotes the language of the claim to the extent that even if the Examiner were correct in his findings, claim 19 would be allowable, because the Examiner has not considered the actual limitations of the claim. The rejection of claim 19 is respectfully traversed.

Claim 1 has been finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,253,291, issued to Pong et al (hereinafter referred to as "Pong") in view of Lai. This ground of rejection is respectfully traversed for the following reasons.

Claim 1 is limited by "a level three cache memory which is directly coupled to at least one memory storage unit". This structure is not found in Pong. Apparently, realizing this failing, the Examiner states:

> ....which is responsively coupled to a level three cache memory which is directly coupled to at least one memory storage [*L3 caches 28, 68, 88, 108 inherently coupled to main memory through system bus 18*; Figs. 2-7];....

This statement is clearly erroneous factually, fails to comply with the controlling law of MPEP 2112, and is legally irrelevant because it does not meet the limitations of the claimed invention.

Their simply is no "main memory" disclosed by Pong. This lack of disclosure alone means that the Examiner has not met his burden of proof under MPEP 2143 of showing that all claimed elements are present in the alleged combination.

Secondly, even if there were a "main memory" within Pong, it is unclear where it would be located within the system. Furthermore, because the alleged L3 memory of Pong is specifically not coupled to system bus 18, the Examiner's statement is clearly erroneous and explicitly inconsistent with the actual disclosure.

Because of these ambiguities, the Examiner cannot possibly meet the requirements of MPEP 2112 which mandates the certainty of "necessity". As a result, even if the Examiner's statement were not clearly erroneously as a matter of fact, it would be incorrect as a matter of controlling law.

Finally, even if the Examiner's statement were factually and legally correct (which it is not), it is legally irrelevant, because it does not meet the requirements of the claim. The claimed invention requires the level two cache memory to be coupled to the level three cache memory via the system bus, and

requires the level three cache memory to be directly coupled to the memory storage unit.

Therefore, the rejection of claim 1, and all claims depending therefrom, is respectfully traversed as based upon clearly erroneous findings of fact, incorrect application of controlling law, and legal irrelevancy for failure to address the actual claim limitations, which are not shown in the references.

Claims 2-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Pone in view of Lai and further in view of U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"). This ground of rejection is respectfully traversed for the following reasons.

As to claim 2, the Examiner states:

> Lynch discloses a second logic which inhibits said first logic from invalidating from mode 3 requests without ownership [*snoop requests checks for the presence of an object in cache only requests for exclusive use which match cache tags are invalidated; there is no invalidate done when there is no hit;* Fig. 4; col. 4, lines 19-20....

Not only is this statement clearly erroneous and a misstatement of the teachings of Lynch, it is legally irrelevant and misconstrues the clear meaning of claim 2. The claim depends from claim 1 and is further limited by "second logic which inhibits said first logic from invalidating for mode 3 requests without ownership". As stated in the specification at page 14, line 22, through page 15, line 2:

> Note that a mode 3 write without ownership means that there is no data within the level one operand cache memory to invalidate.

The point of the "second logic" is to avoid the time delay and resource commitment associated with invalidation when the request is mode 3 without ownership. It is apparent that the Examiner's comments are even less pertinent than the disclosure of Lynch. The rejection of claim 2 is respectfully traversed.

In his rejection of claim 3, the Examiner cites Lynch Fig. 4, and column 4, lines 24-26, for the added limitation. However, this citation of Lynch refers only to the level one (i.e., on-chip cache memories). Column 4, lines 9-10, states:

> Thus, in addition to checking the e-cache in steps 404 and 406, the SIU must check the on-chip caches as well.

Therefore, Lynch does not meet the limitations of claim 3. The rejection is respectfully traversed.

In rejecting claim 4, the Examiner repeats his errors with regard to the rejection of claim 19. Lai, column 6, line 45, through column 7, line 11, temporary stores the "victim line". This is to preserve data from a "flushed" modified cache lime from a store-in cache memory. It is not pertinent to the invention of claim 4. The rejection of claim 4 is respectfully traversed.

Claim 5 depends from claim 1 and is further limited by "fifth logic which determines when said level two cache memory generates a parity error and which in response invalidates said

corresponding level one cache memory location". It should be apparent that the essence of this invention is to invalidate a level one entry in response to a detect parity error in a corresponding level two entry within a system having hierarchical cache memory units.

The Examiner has clearly erroneously found this limitation within Hazawa. He has done so notwithstanding that Hazawa does not disclose a hierarchical cache memory structure. In fact, it is apparent that Hazawa uses (and misuses) the term "level" to refer to a number of things, none of which having anything to do with hierarchical cache memory structures. Furthermore, it is apparent that when Hazawa refers to a "multi-level cache" or a "multi-level register", he means expanded horizontally rather than vertically in a hierarchical fashion.

Even if this were not the case, the Examiner's rejection is based upon clearly erroneous findings of fact. He has cited column 3, lines 38-48, which describes the generation of a "psuedo-error". This "psuedo-error" is "generated" by "diagnostic unit" 1. There is no showing of the generation of a parity error by a level two cache memory.

Even if this were not the case, the claim requires invalidation of a corresponding level one cache memory **location**. There is no showing that Hazawa generates errors in relation to any particular location. The rejection of claim 5 is

respectfully traversed as based upon a plurality of clearly erroneous findings of fact.

Claim 6 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Lai. This ground of rejection is respectfully traversed for the reasons provided below.

In making this rejection, the Examiner repeats a number of the errors discussed above in relation to his rejection of claim 1. He makes the same errors with regard to the differences between the architecture of Pong and the claimed architecture with regard to the level three cache memory, the memory storage unit, and the system bus. These errors were discussed at length above.

In addition, the Examiner repeats his errors with regard to the citation of Lai column 2, lines 41-57. It should be readily apparent that claim 6 is concerned with a local rather than remote write operation. Element f, states:

> a first circuit which invalidates a corresponding portion of said level one cache memory <u>in response to a level one cache memory write hit</u> and a level two cache memory hit. (Emphasis added)

It should be clear that a local write operation is required to generate a level one cache memory write hit. As explained above, the Examiner has already admitted that the cited portion of Lai discusses a remote write operation. The rejection of claim 6, and all claims depending therefrom, is respectfully traversed.

In rejecting claim 9, the Examiner repeats many of the errors associated with his examination of claim 14. The claim is limited by "recording of a data location" whereas the citation in Lai (i.e., column 6, line 45, through column 7, line 11) discusses temporary storage of the "victim line" to be flushed. The rejection of claim 9 is respectfully traversed.

Claims 7 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Lai and further in view of Lynch. This ground of rejection is respectfully traversed for the reasons provided below.

With regard to claim 7, the Examiner repeats many of the errors made in rejecting claim 2. Not only does Lynch not have "second circuit which inhibits said first circuit from said invalidating in response to a mode 3 lack of ownership", the Examiner does not meet the requirements of MPEP 2112 in making his finding of "inherency". The rejection of claim 7 is respectfully traversed as based upon clearly erroneous findings of fact and improper application of controlling law.

In rejecting claim 8, the Examiner states:

> It is clearly <u>obvious</u> that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an <u>inherent</u> feature of any computer system. (Emphasis added)

In accordance with the Examiner's own words, he has established neither "obviousness" (as specified by MPEP 2143) nor "inherency"

(as specified by MPEP 2112). The rejection of claim 8 is respectfully traversed as a matter of law.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Lai and further in view of Hazawa. In making this rejection, the Examiner has repeated many of the errors associated with his rejection of claim 5.

Claim 10 depends from claim 6 and is further limited by:

> a sixth circuit which detects parity errors of said level two cache memory and invalidates said corresponding portion of said level one cache memory in response to said detected parity error

Furthermore, Hazawa has no provision for "invalidating a corresponding portion of level on cache memory in response to said detected parity error". Parity checkers 31, 32, 33, and 34 of Hazawa, even if equivalent to the claimed "sixth circuit" cannot have any impact on invalidation of any portion of another level of cache memory. The rejection of claim 10 is respectfully traversed.

Claims 12-13 and 17-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Lynch. This ground of rejection is respectfully traversed for the reasons provided below.

In rejecting claims 12 and 17, the Examiner repeats many of the errors made in the rejection of claim 2. Lynch simply does not have the claimed structure. Furthermore, the Examiner admits that it does not and suggests that the structure is inherent.

However, the Examiner does not even attempt to meet his burden of proof under MPEP 2112. The rejection of claims 12 and 17 is respectfully traversed.

In rejecting claims 13 and 18, the Examiner again finds obviousness without meeting the requirements of MPEP 2143 and finds inherency without meeting the requirements of MPEP 2112. The rejection of claims 13 and 18 is respectfully traversed.

Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Hazawa. Claim 15, for example, requires detecting a parity error. Hazawa has no such teaching. More important is the invalidation of a corresponding portion of the level one cache memory. There is no showing that Hazawa can invalidate a portion of any cache memory. The rejection of claim 20 is similarly defective. The rejection of claims 15 and 20 is respectfully traversed.

Claim 21 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Hazawa. This ground of rejection is respectfully traversed for the following reasons. Hazawa discusses only "psuedo-errors". There is no showing of any actual parity error in Hazaw. Furthermore, there is no showing of the invalidation of any data element as a result thereof. The rejection of claim 21, and all claims depending therefrom is respectfully traversed.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Hazawa and further in view of Lynch. This ground of rejection is respectfully traversed for the following reasons.

In making his rejection, the Examiner alleges the combination of the embodiment of Fig. 2 of Pong with the embodiment of Lynch described at column 3, lines 43-48. This alleged combination is specifically not motivated and is actually taught against by the references. Pong describes Fig. 2 at column 3, line 43-45, stating:

> FIG. 2 is a block diagram of an **inclusive** asynchronous cache multiprocessor system suitable for use according to the present invention. (Emphasis added)

Lynch, on the other hand, describes his disclosure in the title stating:

> **NON-INCLUSIVE** CACHE METHOD USING PIPELINED SNOOP BUS (emphasis added)

It is apparent that one of skill in the art would be sufficiently knowledgeable that he/she would not attempt to utilize the **non-inclusive** cache method of Lynch with the **inclusive** cache system of Pong. The rejection of claim 22 is respectfully traversed.

Claims 23-25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Pong in view of Hazawa and further in view of Lynch and yet further in view of Lai. This ground of rejection is respectfully traversed for the reasons provided below.

In addition to the lack of motivation of making the alleged combination of "inclusive", "non-inclusive", "partially inclusive", and "exclusive" cache memory techniques, the alleged combination does not meet the limitations of the claimed invention.

Specifically, as to claim 23, the Examiner repeats his error by confusion the SNOOP hit of Lai column 2, lines 41-57, with the claimed local memory request hit. He repeats many of the other errors in his rejection of claims 24 and 25. The rejection of claims 23-25 is respectfully traversed.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Please charge any deficiencies or credit any overpayment to Deposit Account No. 14-0620.

Respectfully submitted,

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By his attorney,

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